

## Chapter 4

# Spacecraft Test Techniques

Spacecraft and systems should be subjected to transient upset tests to verify immunity. It is the philosophy in this document that testing is an essential ingredient in a sound spacecraft charging protection program. In this Chapter, the philosophy and methods of testing spacecraft and spacecraft systems are reviewed. It is largely unchanged from the analogous section in NASA TP-2361 [1].

### 4.1 Test Philosophy

The philosophy of an ESD test is identical to that of other environmental qualification tests:

- a. Subject the spacecraft to an environment representative of that expected.
- b. Make the environment applied to the spacecraft more severe than expected as a safety margin to give confidence that the flight spacecraft will survive the real environment.
- c. Have a design qualification test sequence that is extensive and includes the following:
  - 1) Test of all units of hardware.
  - 2) Use of long test durations.
  - 3) Incorporation of as many equipment operating modes as possible.
  - 4) Application of the environment to all surfaces of the test unit.

- d. Have a flight hardware test sequence of more modest scope, such as deleting some units from test if qualification tests show great design margins; use shorter test durations; use only key equipment operating modes; and apply the environment to a limited number of surfaces.

Ideally, both prototype and flight spacecraft should be tested in a charging simulation facility. They should be electrically isolated from ground and bombarded with electron, ion, and EUV radiation levels corresponding to substorm environment conditions. Systems should operate without upset throughout this test. Generally, there is a reluctance to subject flight hardware to this kind of test. One good reason is the possibility of latent damage, i.e., internal physical damage to circuitry that apparently still functions but that has weakened the hardware and may lead to later failure. For that reason, flight hardware is ESD tested less frequently than developmental hardware. For the same reason, flight hardware might be subjected to lower test amplitudes as a precaution to demonstrate survivability but without margin.

Because of the difficulty of simulating the actual environment (space vacuum and plasma parameters, including species such as ions, electrons, and heavier ions; mean energy; energy spectrum; and direction), spacecraft charging tests usually take the form of assessing unit immunity to electrical discharge transients. The appropriate discharge sources are based on separate estimates of discharge parameters.

Tests at room ambient temperature using radiated and injected transients are more convenient. These ground tests, however, cannot simulate all the effects of the real environment because the transient source may not be in the same location as the region that may discharge and because a spark in air has a slower risetime than a vacuum arc. The sparking device's location and pulse shape must be analyzed to provide the best possible simulation of coupling to electronic circuits. To account for the difference in risetime, the peak voltage might be increased to simulate the  $dV/dt$  (time rate of change of the voltage) parameter of a vacuum arc. Alternatively, the voltage induced during a test could be measured and the in-flight noise extrapolated from the measured data.

There are no simple rules to be followed in determining whether or how much to test. General guidance dictates that an engineering version of the hardware be tested in lieu of the flight hardware and that this testing has margins that are more severe than the expected environment. The trade-offs are common to other environmental testing; the main difference is that the ESD- and IESD-specific threats are more difficult to replicate in practical tests than for other environmental disciplines.

The dangers in not testing are that serious problems related to surface or internal charging will go undetected and that these problems will affect the survivability of the spacecraft. The best that can be done in the absence of testing is good design supplemented by analysis. Good IESD and surface charging design techniques are always appropriate, no matter what the overt environmental threat is, and should be followed as a necessary precaution in all cases.

A proper risk assessment involves a well-planned test, predictions of voltage stress levels at key spacecraft components, verification of these predictions during test, checkout of the spacecraft after test, and collaboration with all project elements to coordinate and assess the risk factors.

## 4.2 Simulation of Parameters

Because ESD test techniques are not well established, it is important to understand the various parameters that must be simulated, at a minimum, to perform an adequate test. On the basis of their possibility of interference to the spacecraft, the following items should be considered in designing tests:

- a. Spark location.
- b. Radiated fields or structure currents.
- c. Area, thickness, and dielectric strength of the material.
- d. Total charge involved in the event.
- e. Breakdown voltage.
- f. Current waveform (risetime, width, falltime, and rate of rise (in amperes per second)).
- g. Voltage waveform (risetime, width, falltime, and rate of rise (in volts per second)).

Table 4-1 (Ref. [1] with corrections) shows typical values calculated for representative spacecraft. The values listed in this table were compiled from a variety of sources, mostly associated with the Voyager and Galileo spacecraft. The values for each item, e.g., those for the dielectric plate, have been assembled from the best available information and made into a more or less self-consistent set of numbers. The process is described in the footnotes to Table 4-1. References [2] and [3] contain further description and discussion.

**Table 4-1. Examples of estimated space-generated ESD spark parameters.**

<b>ESD Generator</b>	<b>C (nF) (1)</b>	<b>Vb (kV) (2)</b>	<b>E (mJ) (3)</b>	<b>Ipk (A) (4)</b>	<b>TR (ns) (5)</b>	<b>TP (ns) (6)</b>
Dielectric plate to conductive substrate	20	1	10	2 (7)	3	10
Exposed connector dielectric	0.150	5	1.9	36	10	15
Paint on high-gain antenna	300	1	150	150	5	2400
Conversion coating on metal plate (anodize)	4.5	1	2.25	16	20	285
Paint on optics hood	550	0.360	36	18	5	600

Notes:

1. Capacitance computed from surface area, dielectric thickness, and dielectric constant.
2. Breakdown voltage computed from dielectric thickness and material breakdown strength.
3. Energy computed from  $E = 1/2 CV^2$ .
4. Peak current estimated based on measured data; extrapolation based on square root of area.
5. Discharge current risetime measured and deduced from test data.
6. Discharge current pulse width to balance total charge on capacitor.
7. Replacement current in longer ground wire; charge is not balanced.

## 4.3 General Test Methods

### 4.3.1 ESD-Generating Equipment

Several representative types of test equipment are tabulated in Table 4-2 (Ref. [1] with corrections) and described later. Where possible, typical parameters for that type of test are listed.

**Table 4-2. Examples of several ESD sources.**

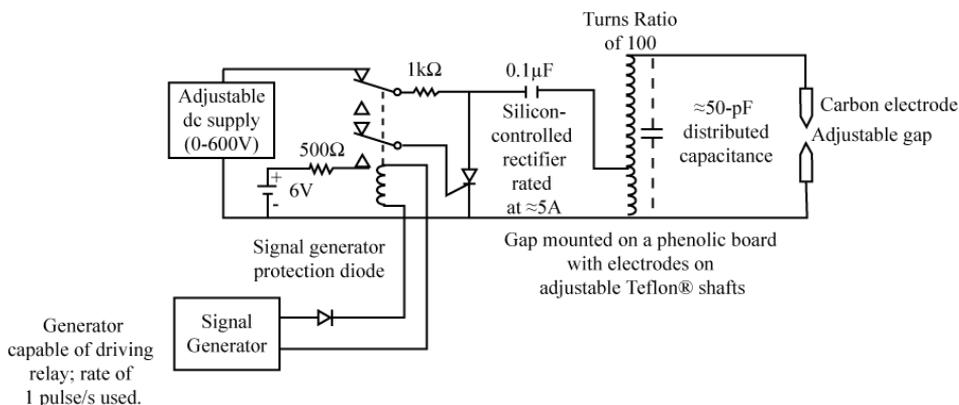
<b>ESD Generator Test Simulation</b>	<b>C (nF)</b>	<b>Vb (kV)</b>	<b>E (mJ)</b>	<b>Ipk (A)</b>	<b>TR (ns)</b>	<b>TP (ns)</b>
MIL-STD-1541A (auto coil) (1)	0.035	19	6	80	5	20
Flat plate 20 cm × 20 cm at 5 kV, 0.8 mm (3 mil) Mylar® insulation	14	5	180	80	35	880
Flat plate with lumped-element capacitor	550	0.450	56	15	15	(2)
Capacitor direct injection	1.1	0.32	0.056	1	3-10	20
Capacitor arc discharge	60	1.4	59	1000	(3)	80
Commercial ESD tester	0.15	20	30	130	5	22

Notes:

1. Parameters were measured on one unit similar to the MIL-STD-1541A, *Electromagnetic Compatibility Requirements for Space Systems* [4], design.
2. RC time constant decay can be adjusted with an external resistor in the circuit.
3. Value uncertain.

### 4.3.1.1 MIL-STD-1541A Arc Source

The schematic and usage instructions for the MIL-STD-1541A [4] arc source are presented in Fig. 4-1. The arc source can be manufactured relatively easily and can provide the parameters necessary to simulate a space-caused ESD event. The only adjustable parameter for the MIL-STD-1541A [4] arc source, however, is the discharge voltage achieved by adjusting the discharge gap and, if necessary, the adjustable dc supply to the discharge capacitor. As a result, peak current and energy vary with the discharge voltages. Since the risetime, pulse width, and falltime are more or less constant, the voltage and current rates of rise and fall are not independent parameters. This permits some degree of flexibility in planning tests but not enough to cover all circumstances. Recent versions of MIL-STD-1541 [4] no longer reference this test method.



Typical Gap-Spacing and Voltage Breakdown (Vb) Levels

Gap (mm)	Vb (kV)	Approximate Energy Dissipated (μJ)
1	1.5	56.5
2.5	3.5	305
5	6	900
7.5	9	2000

Fig. 4-1. MIL-STD-1541A[4] arc source.

#### 4.3.1.2 *Flat-Plate Capacitor*

A flat-plate capacitor made of aluminum foil over an insulator can be used in several circumstances. Examples of spacecraft areas that can be simulated by a flat-plate capacitor are thermal blanket areas, dielectric areas such as calibration targets, and dielectric areas such as non-conductive paints. The chief value of a flat-plate capacitor is to permit a widespread discharge to simulate the physical path of current flow. This can be of significance where cabling or circuitry is near the area in question. Also, the larger size of the capacitor plates allows them to act as an antenna during discharge, producing significant radiated fields.

Table 4-2 shows one example of the use of a flat-plate capacitor. Several parameters can be varied, chiefly the area and the dielectric thickness; both of these affect the capacitance, the discharge current, and the energy. The discharge voltage of the flat plate can be controlled by using a needle-point discharge gap at its edge that is calibrated to break down before the dielectric. This gap also affects discharge energy. In this manner, several mechanical parameters can be designed to yield discharge parameters more closely tailored to those expected in space.

The difficulties of this method include the following:

- a. The test capacitor is usually not as close to the interior cabling as the area it is intended to simulate (e.g., it cannot be placed as close as the paint thickness).
- b. The capacitance of the test capacitor may be less than that of the area it is intended to simulate. To avoid uncontrolled dielectric breakdown in the test capacitor, its dielectric may have to be thicker than the region it simulates. If so, the capacitance will be reduced. The area of the test capacitance can be increased to compensate, but then the size and shape will be less realistic.

#### 4.3.1.3 *Lumped-Element Capacitors*

Use of lumped-element capacitors (off-the-shelf, manufactured capacitors) can overcome some of the objections raised about flat-plate capacitors. They can have large capacitances in smaller areas and thus supplement a flat-plate capacitor if it alone is not adequate. The deficiencies of lumped-element capacitors are as follows:

- a. They generally do not have the higher breakdown voltages (greater than 5 kV) needed for ESD tests.

- b. Some have a high internal resistance and cannot provide the fast risetimes and peak currents needed to simulate ESD events.

Generally, the lumped–element capacitor discharge would be used most often in lower voltage applications to simulate painted or anodized surface breakdown voltages and in conjunction with the flat-plate capacitors.

#### 4.3.1.4 *Other Source Equipment*

Reference [5] describes several other similar types of ESD simulators. It is a useful document if further descriptions of ESD testing are desired.

#### 4.3.1.5 *Switches*

A wide variety of switches can be used to initiate the arc discharge. At low voltages, semiconductor switches can be used. The MIL-STD-1541A [4] arc source uses a silicon controlled rectifier (SCR) to initiate the spark activity on the primary of a step-up transformer; the high voltage occurs at an air spark gap on the transformer's secondary. Also at low voltages, mechanical switches can be used, e.g., to discharge modest-voltage capacitors. The problem with mechanical switches is their bounce in the early milliseconds. Mercury-wetted switches can alleviate this problem to a degree.

For high-voltage switching in air, a gap made of two pointed electrodes can be used as the discharge switch. Place the tips pointing toward each other and adjust the distance between them to about 1 mm/kV of discharge voltage. The gap must be tested and adjusted before the test, and it must be verified that breakdown occurred at the desired voltage. For tests that involve varying the amplitude, a safety gap connected in parallel is suggested. The second gap should be securely set at the maximum permissible test voltage. The primary gap can be adjusted during the test from zero to the maximum voltage desired without fear of inadvertent overtesting. Do the test by charging the capacitor (or triggering the spark coil) and relying on the spark gap to discharge at the proper voltage.

The arc source's power supply must be isolated sufficiently from the discharge so that the discharge is a transient and not a continuing arc discharge. A convenient test rate is once per second. To accomplish this rate, it is convenient to choose the capacitor and isolation resistor's resistance-capacitance time constant to be about 0.5 s and to make the high-voltage power supply output somewhat higher than the desired discharge voltage.

For tests that involve a fixed discharge voltage, gas discharge tubes are available with fixed breakdown voltages. The advantage of the gas discharge tube over needle points in air is its faster risetime and its very repeatable

discharge voltage. The gas discharge tube's dimensions (5 to 7 cm or longer) can cause more RF radiation than a smaller set of needle-point air gaps.

Another type of gas discharge tube is the triggered gas discharge tube. This tube can be triggered electronically, much as the gate turns on a silicon-controlled rectifier (SCR). This method has the added complexity of the trigger circuitry. Additionally, the trigger circuitry must be properly isolated so that discharge currents are not diverted by the trigger circuits.

### **4.3.2 Methods of ESD Applications**

The ESD energy can range from very small to large (as much as 1 J but usually millijoules). The methods of application can range from indirect (radiated) to direct (applying the spark directly to a piece part). In general, the method of application should simulate the expected ESD source as much as possible. Several typical methods are described here.

#### **4.3.2.1 Radiated Field Tests**

The sparking device can be operated in air at some distance from the component. This technique can be used to check for RF interference to communications or surveillance receivers as coupled into their antennas. It can also be used to check the susceptibility of scientific instruments that may be measuring plasma or natural radio waves. Typical RF-radiated spectra are shown in Fig. 4-2.

#### **4.3.2.2 Single-Point Discharge Tests**

Discharging an arc onto the spacecraft surface or a temporary protective metallic fitting with the arc current return wire in close proximity can represent the discharge and local flowing of arc currents. This test is more severe than the radiated test, since it is performed immediately adjacent to the spacecraft rather than some distance away.

This test simulates only local discharge currents; it does not simulate blow-off of charges which cause currents in the entire structure of the spacecraft.

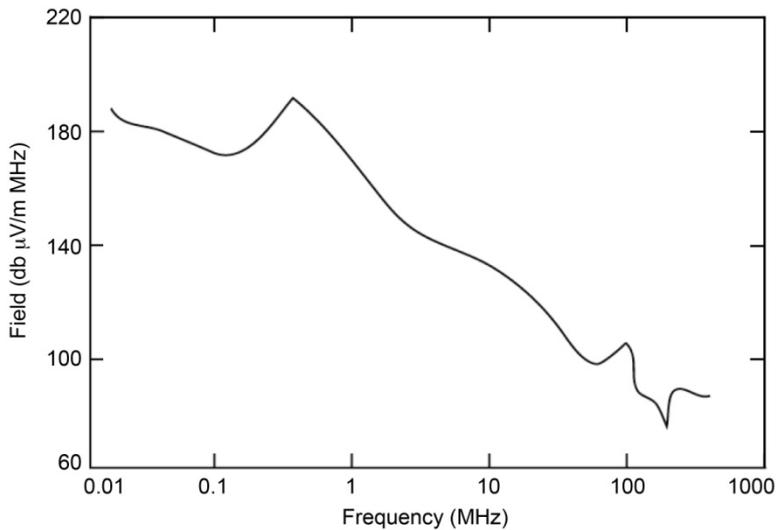


Fig. 4-2. Typical RF-radiated fields from MIL-STD-1541A [4] arc sources.

#### 4.3.2.3 Structure Current Tests

The objective of structure current testing is to simulate blow-off of charges from a spacecraft surface. If a surface charges and a resultant ESD occurs, the spark may vaporize and mechanically remove material and charges without local charge equalization. In such a case, the remaining charge on the spacecraft will redistribute itself and cause structural currents.

Defining the actual blow-off currents and the paths they take is difficult. Nevertheless, it is appropriate to do a structure current test to determine the spacecraft susceptibility, using test currents and test locations supported by analysis as illustrated in Section 4.2 and Table 4-1. Typically, such a test would be accomplished by using one or more of the following current paths (Fig. 4-3):

- a. Diametrically opposed locations (through the spacecraft).
- b. Protuberances (from landing foot to top, from antenna to body, and from thruster jets to opposite side of body).
- c. Extensions or booms (from end of sensor boom to spacecraft chassis and from end of solar panel to spacecraft chassis).
- d. From launch attachment point to other side of spacecraft.

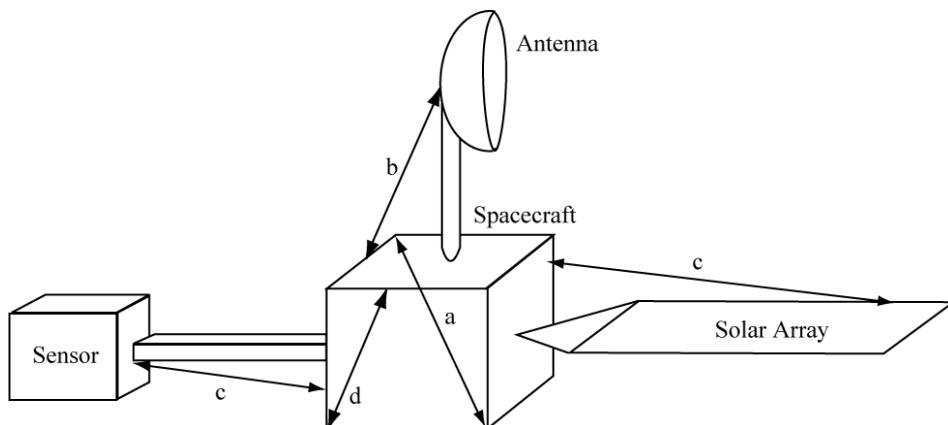


Fig. 4-3. Paths for ESD currents through structure.

The tests using current paths “a” and “d” are of a general nature. Tests using current paths “b” and “c” simulate probable arc locations on at least one end of the current path. These test points include thrusters, whose operation can trigger an incipient discharge, and also landing feet and the attachment points, especially if used in a docking maneuver, when they could initiate a spark to the mating spacecraft.

Test “c” is an especially useful test. Solar panels often have glass (non-conductive) cover slides, and sensors may have optics (non-conductive) that can cause an arc discharge. In both cases, any blow-off charge would be replaced by a current in the supporting boom structure that could couple into cabling in the boom. This phenomenon is possibly the worst-case event that could occur on the spacecraft because the common length of the signal or power cable near the arc current is the longest on the spacecraft.

#### 4.3.2.4 Unit Testing

**4.3.2.4.1 General.** Unit ESD testing serves the same purpose as it serves in standard environmental testing, i.e., it identifies design deficiencies at a stage when the design is more easily changed. It is, however, very difficult to provide a realistic determination of the unit’s environment as caused by an ESD on the spacecraft.

A unit testing program could specify a single ESD test for all units or could provide several general categories of test requirements. The following test categories are provided as a guide:

- a. Internal units (general) must survive, without damage or disruption, the MIL-STD-1541A [4] arc source test (discharges to the unit but no arc currents through the unit's chassis).
- b. External units mounted outside the Faraday cage (usually exterior sensors) must survive the MIL-STD-1541A [4] arc source at a 5 kV level with discharge currents passing from one corner to the diagonally opposite corner (four pairs of locations).
- c. For units near a known ESD source (e.g., solar cell cover slides and Kapton® thermal blankets), the spark voltage and other parameters must be tailored to be similar to the expected spark from that dielectric surface. For solar cells, it is important that the arc injection point be at the edge of a cell, rather than at an interconnect or bypass diode. This is because the solar cell damage happens because of high current densities at cell edges, rather than because of currents flowing through the cell.

**4.3.2.4.2 Unit Test Configuration.** ESD tests of the unit (subsystem) can be performed with the subsystem configured as it would be for a standard EMC-radiated susceptibility test. The unit is placed on and electrically bonded to a grounded copper-topped bench. The unit is cabled to its support equipment, which is in an adjacent room. The unit and cabling should be of flight construction with all shields, access ports, etc., in flight condition. All spare cables should be removed.

**4.3.2.4.3 Unit Test Operating Modes.** The unit should be operated in all modes appropriate to the ESD arcing situation. Additionally, the unit should be placed in its most sensitive operating condition (amplifiers in highest gain state, receivers with a very weak input signal) so that the likelihood of observing interference from the spark is maximized. The unit should also be exercised through its operating modes to assure that mode change commands are possible in the presence of arcing.

#### **4.3.2.5 Spacecraft Testing**

The system-level test will provide the most reliable determination of the expected performance of a space vehicle in the charging environment. Such a test should be conducted on a representative spacecraft before exposing the flight spacecraft to ensure that there will be no inadvertent overstressing of flight units.

A detailed test plan must be developed that defines test procedures, instrumentation, test levels, and parameters to be investigated. Test techniques will probably involve current flow in the spacecraft structure. Tests can be conducted in ambient environments, but screen rooms with electromagnetic

dampers are recommended. MIL-STD-1541A [4] system test requirements and radiated EMI testing are considered to be a minimal sequence of tests.

The spacecraft should be isolated from ground. Instrumentation must be electrically screened from the discharge test environment and must be carefully chosen so that instrument response is not confused with spacecraft response. The spacecraft and instrumentation should be on battery power. Complete spacecraft telemetry should be monitored. Voltage probes, current probes, E and H field current monitors, and other sensors should be installed at critical locations. Sensor data should be transmitted with fiber-optic data links for best results. Oscilloscopes and other monitoring instruments should be capable of resolving the expected fast response to the discharges (usually less than 250 MHz frequency content).

The test levels should be determined from analysis of discharging behavior in the substorm environment. It is recommended that full level testing, with test margins, be applied to structural, engineering, or qualification models of spacecraft with only reduced levels applied to flight units. The test measurements, e.g., structural currents, harness transients, and upsets, are the key system responses that are to be used to validate predicted behavior.

**4.3.2.5.1 General.** Spacecraft testing is generally performed in the same fashion as unit testing. A test plan of the following sort is typical (see Fig. 4-3):

- a. The MIL-STD-1541A [4] radiated test is applied around the entire spacecraft.
- b. Spark currents from the MIL-STD-1541A [4] arc source are applied through spacecraft structure from launch vehicle attachment points to diagonally opposite corners.
- c. ESD currents are passed down the length of booms with cabling routed along them, e.g., sensor booms or power booms. Noise pickup into cabling and circuit disruption are monitored.
- d. Special tests are devised for special situations. For example, dielectric regions, such as quartz second-surface mirrors, Kapton<sup>®</sup> thermal blankets, and optical viewing windows should have ESD tests applied on the basis of their predicted ESD characteristics.

Examples of system level ESD current injection test results are shown in Fig. 4-4. The MIL-STD-1541A [4] ESD waveform generator was measured directly with very short leads on the output. The peak current is about 66 A,

risetime about 5.2 ns, and a time base of 20 nanoseconds per division (ns/div). The waveform was measured during a system-level test. The current was applied via 9 m of attachment wiring (two 4.5-m lengths) from the same MIL-STD-1541A [4] sparker to the top of a spacecraft, with the current return at the solar array drive on the body of the spacecraft. Because of inductance in the long leads, the risetime has increased to 40 ns, the peak current is now 15 A, and the time base is 200 ns/div. (Scale factors in these historic pictures are different in each picture and include attenuations and probe factors.)

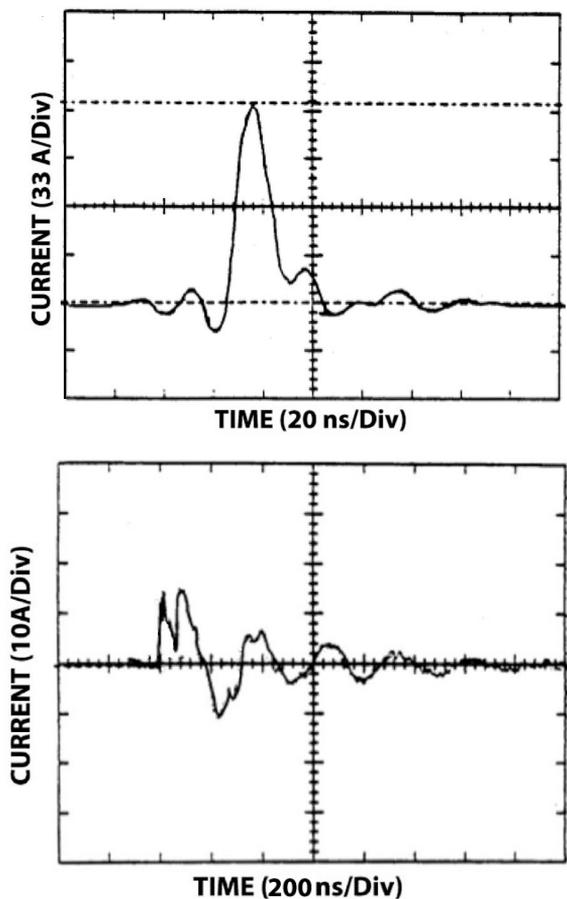


Fig. 4-4. Examples of system level ESD test waveforms (units of time and current are noted per division ["Div"] tic mark).

**4.3.2.5.2 Spacecraft Test Configuration.** The spacecraft ESD testing configuration ideally simulates a 100-percent flight-like condition. This may be difficult because of the following considerations:

- a. Desire for ESD diagnostics in the spacecraft.
- b. Non-realistic power system (no solar array).
- c. Local rules about grounding the spacecraft to facility ground.
- d. Cost and schedules to completely assemble the spacecraft for the test and later disassemble it if failures or anomalies occur.
- e. The possible large capacitance to ground of the spacecraft in its test fixture.
- f. ESD coupling onto non-flight test cabling.
- g. A fear of immediate or latent damage to the spacecraft.

**4.3.2.5.3 Test Diagnostics.** To obtain more information about circuit response than can be obtained by telemetry, it is common to use an oscilloscope to measure induced voltages related to the ESD test sparks at key circuits. If improperly implemented, the very wires that access the circuits and exit the spacecraft to test equipment (e.g., oscilloscopes) will act as antennas and show noise that never would be present without those wires.

Two approaches have been used with some success. The first is using conventional oscilloscope probes with great care. Long oscilloscope probes (3 m) were procured from Tektronix. For the circuits being monitored, a small tee breakout connector was fabricated and inserted at the connector nearest the circuit. Two oscilloscope probes were attached to each circuit's active and return wires, and the probe tips were grounded to satellite structure in the immediate vicinity of the breakout tee. The probe grounds were less than 15 cm from the probe tip. The signal was measured on a differential input of the oscilloscope. Before installation, the probes were capacitively compensated to their respective oscilloscope preamplifiers, and it was verified that their common-mode voltage rejection was adequate (normal good practice). The two probe leads were twisted together and routed along metal structure inside the satellite until they could be routed out of the main chassis enclosure. They were then routed (still under thermal blankets) along the structure to a location as remote as possible from any ESD test location and finally routed to the oscilloscope. The oscilloscopes were isolated from building ground by isolation transformers. Clearly, this method permits monitoring only a few circuits [3].

A second method of monitoring ESD-induced voltage waveforms on internal circuits is the use of battery-powered devices that convert voltages to light-emitting diode (LED) signals. The LED signals can be transmitted by fiber optics to exterior receiving devices, where the voltage waveform is reconstructed. As with the oscilloscope probes, the monitoring device must be attached to the wires carefully with minimal disturbance to circuit wiring. The fiber-optic cable must be routed out of the satellite with minimal disturbance. The deficiency of such a monitoring scheme is that the sending device must be battery powered, turned on, and installed in the spacecraft before spacecraft buildup; and it must operate for the duration of the test. The need for batteries and the relatively high-power consumption of LED interface circuits severely restrict this method.

Another proposed way to obtain circuit response information is to place peak-hold circuitry (tattle-tales) at key circuit locations, installed as described above. This method is not very useful because the only datum presented is that a certain peak voltage occurred. There is no evidence that the ESD test caused it, and there is no way to correlate that voltage with any one of the test sequences. For analysis purposes, such information is worthless.

**4.3.2.5.4 Use of External (Non-Flight) Power Supplies.** Spacecraft using solar cells or nuclear power supplies often must use support equipment (SE) power supplies for ground test activities and thus are not totally isolated from ground. In such cases, the best work-around is to use an isolated and balanced output power supply with its wires routed to the spacecraft at a height above ground to avoid stray capacitance to ground. The power wires should be shielded to avoid picking up stray radiated ESD noise; the shields should be grounded at the SE end of the cable only.

**4.3.2.5.5 Facility Grounding.** To simulate flight, the spacecraft should be isolated from ground. Normal test practice dictates an excellent connection to facility ground. For the purpose of the ESD test, a temporary ground of 0.2 to 2 M $\Omega$  or more will isolate the spacecraft. Generally 0.2 to 2 M $\Omega$  is sufficient grounding for special test circumstances of limited duration and can be tolerated by the safety or QA organization for the ESD test.

**4.3.2.5.6 Cost and Schedules to Assemble and Disassemble Spacecraft.** Often testing is done in the most compact form possible, attempting to interleave several tasks at one time or to perform tasks in parallel. This practice is incompatible with the needs of ESD testing and must be avoided. A thermal-vacuum test, for example, is configured like the ESD test but has numerous (non-flight) thermocouple leads penetrating from the interior to the exterior of the spacecraft. These leads can act as antennas and bring ESD-caused noise into

satellite circuitry where it never would have been. Dynamic (shake table) test configurations have the same problem with the accelerometers.

**4.3.2.5.7 Spacecraft Capacitance to Ground during Test.** If stray capacitance to facility ground is present during the ESD test, it will modify the flow of ESD currents. For a better test, the spacecraft should be physically isolated from facility ground. It can be shown that raising a 1.5 m diameter spherical satellite 0.5 m off the test flooring reduces the stray capacitance nearly to that of an isolated satellite in free space. A dielectric (e.g., wood) support structure can be fabricated for the ESD test and will provide the necessary capacitive isolation.

**4.3.2.5.8 ESD Coupling onto Non-Flight Test Cabling.** One method of reducing ESD coupling to and from the spacecraft on non-flight test wiring is the use of ferrite beads on all such wiring. The most realistic approach is to have no non-flight cabling, leaving only information that would be visible while in flight, at the expense of extra diagnostic information.

## References

- [1] C. K. Purvis, H. B. Garrett, A. C. Whittlesey, and N. J. Stevens, *Design Guidelines for Assessing and Controlling Spacecraft Charging Effects*, NASA Technical Paper 2361, National Aeronautics and Space Administration, September 1984.

This document has been widely used by practitioners of this art (usually EMC engineers or radiation survivability engineers) since its publication in 1984. Its contents are limited to surface charging effects. The contents are valid to this day for that purpose. NASA TP-2361 contents have been incorporated into this NASA-STD-4002, Rev A, with heavy editing. Many of the original details, especially time-variant and multiple-case versions of suggested environments, have been simplified into single worst-case environments in NASA-HDBK-4002, Revision A. Some background material has not been transferred into this document, so the original may still be of interest.

- [2] P. L. Leung, G. H. Plamp, and P. A. Robinson, Jr., “Galileo Internal Electrostatic Discharge Program,” *Spacecraft Environmental Interactions Technology 1983*, October 4–6, Colorado Springs, Colorado, NASA CP-2359/AFGL-TR-85-0018, National Aeronautics and Space Administration, pp. 423–435, 1983.

This paper, documented in the 1985 publication and presented at the 4th Spacecraft Charging Technology Conference, describes a very neat and clear test that measures the effect of line lengths and circuit board metal areas in the resultant ESD amplitude. It also measures the amplitude of

ESD transients from electron beam charging on 50  $\Omega$  loads from various conductors.

- [3] A. C. Whittlesey, "Voyager Electrostatic Discharge Protection Program," presented at *IEEE International Symposium on EMC*, Atlanta, Georgia, pp. 377–383, 1978.
- [4] *Electromagnetic Compatibility Requirements for Space Systems*, MIL-STD-1541A (USAF), United States Air Force, 42 pages, December 30, 1987.
- [5] J. M. Wilkenfeld, B. L. Harlacher, and D. Mathews, *Development of Electrical Test Procedures for Qualification of Spacecraft against EID*, Vol. II, *Review and Specification of Test Features*, NASA CR-165590, National Aeronautics and Space Administration, April 1982.  
EID refers to electron-induced discharge, a term used in those days. A very good survey of spacecraft ESD test methodology as of 1982. Includes the methods used for several satellite systems and provides a comparison and evaluation of their relative merits. This is a fundamental document for anyone in the spacecraft ESD test business.

