

A 250MHz CMOS Bandpass Delta Sigma Modulator Using Continuous-Time Resonator Structure (Short Paper)

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ABSTRACT

In this paper, the design of a CMOS fourth-order bandpass Delta-Sigma modulator clocking at 1GHz for direct conversion of narrowband signals located at 250 MHz is presented. The continuous-time loop filter is based on two on-chip parallel LC tanks. Q-enhancement transconductors are connected as negative resistors to cancel the positive resistance of the on-chip low quality factor inductors. The modulator is implemented in a 0.35um triple-metal standard analog CMOS technology and occupies about 1.0 mm² with the two on-chip inductors consuming about 60% of the total area. Post-layout simulation in CADENCE environment demonstrates the modulator achieves a 46.86dB (~7.5-bit) performance in a 15.6MHz bandwidth corresponding to an over-sampling ratio of 64.

1. INTRODUCTION

Bandpass delta sigma A/D converters perform direct conversion of a RF or IF narrow band signal to digital for processing and heterodyning in digital domain. The ability of performing narrowband conversion at a frequency other than DC makes them particularly attractive for radio applications: with the IF filters pushed to the digital side, testing becomes systematic and changing filter coefficients becomes easy, while digital programmability allows a single radio to adapt to different country standards or different communication systems. These benefits would make the overall system becomes power efficient.

The majorities of delta-sigma modulators in the literature are implemented as discrete-time circuits such as switched-capacitor [1][2] or switched-current circuits[3]. However, the speed of these modulators is limited, both by OPAMP bandwidth and by the fact that the circuit waveforms need several clock periods to settle. To reduce the settling time of the OPAMP, the cost of higher power dissipation and larger size must be paid.

The idea of using continuous-time filters in delta sigma modulators which eliminates the need of high speed OPAMPs was developed to relax the clock rate restrictions [4] and in recent years clocking rates in the gigahertz range

were reported [5][6]. To achieve such a high speed data conversion, these modulators were realized using RF transistors such as in GaAs or InP technologies, and were hard to be integrated on the same chip with digital signal processing modules which are prevalingly realized in standard CMOS technology. On the other hand, attempts in CMOS bandpass delta sigma modulators are still limited to IFs of tens of megahertz [7][8].

In our work, we designed a 0.35um CMOS fourth-order bandpass continuous-time delta sigma modulator clocking at 1-GHz for direct conversion of narrowband signals located at 250 MHz. In the following sections, we will discuss how the system structure is designed and how we address the difficulties commonly encountered in continuous-time delta-sigma modulators, such as excess loop delay, clock feed-through problem and metastability effects, and then post-layout simulation results are given to validate the performance of the design.

2. SYSTEM ARCHITECTURE

Continuous-time (CT) implementation of delta-sigma modulators can normally operate at a much higher frequency than their discrete-time (DT) counterpart, but the design of a CT delta sigma modulator is basically designed by transforming a DT prototype into a CT system, since there is a great deal of literature and software available to help us choosing the DT loop filter $H(z)$ that will meet the

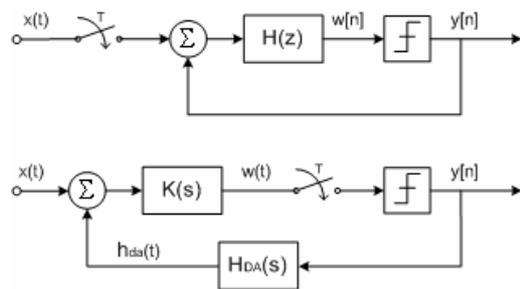


Fig. 1. Mapping between DT and CT systems

given specification. The principle of this transformation is illustrated in Fig. 1, where $h_{da}(t)$ is the feedback signal in the CT system. The transfer function of the CT system $K(s)$ should be chosen in such a way that the quantizer inputs at sampling instants are identical in both systems, i.e. $w(nT) = w[n]$, then a CT equivalent can be found through:

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$$Z^{-1}\{H(z)\} = L^{-1}\{H_{DA}(s)K(s)\}|_{t=nT_s} \quad (1)$$

This transformation between DT and CT is called the impulse-invariant transformation [9].

In our design, we start with a simple second-order lowpass DT delta sigma modulator whose loop filter is

$$H_{LP2}(z) = \frac{-2z^{-1} + z^{-2}}{(1 - z^{-1})^2},$$

since it is stable as long as the input amplitude is smaller than that of its quantizer feedback. Higher-order modulators usually become unstable before quantizer feedback amplitude is reached. Performing the substitution of $z^{-1} \rightarrow -z^{-2}$ on a low pass delta sigma modulator will move the noise notch from dc to $f_s/4$, one-quarter the sampling frequency, while maintaining the stability properties and doubling the order. By doing this to $H_{LP2}(z)$, we get our fourth order bandpass DT prototype

$$H_{BP4}(z) = \frac{2z^{-2} + z^{-4}}{(1 + z^{-2})^2} = z^{-1} \frac{2z^{-1} + z^{-3}}{(1 + z^{-2})^2}. \quad (2)$$

To derive our continuous time delta sigma modulator, we apply the DT-to-CT transformation (1) to our DT prototype design (2). As we can see from equation (1), the actual DAC feedback waveform $H_{DA}(s)$ is critical in determining the loop filter $K(s)$. If we use only one DAC with a Return-to-Zero (RZ) waveform (Fig. 5), the DT-to-CT transformation (1) yields

$$K(s) = \frac{-2.146s^3 + 0.3906s^2 - 4.062s + 5.642}{(s^2 + (\mathbf{p}/2)^2)^2} \quad (3)$$

We have four numerator coefficients in $K(s)$ to control, but we have only two tunable parameters (K1 and K2). The design as shown in Fig. 2 suffers from lack of controllability.

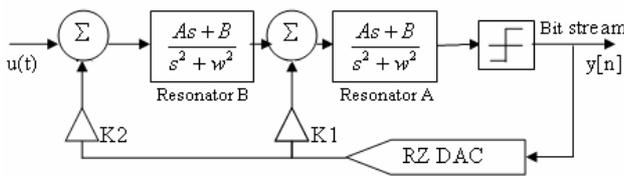


Fig. 2 Controllability problem with single DAC

In order to maintain full controllability of the continuous-time modulator to keep it equivalent to its prototype discrete-time design, the multi-feedback architecture [10][11] is adopted. Both Return-to-Zero (RZ) and Half-delayed Return-to-Zero (HRZ) feedback waveforms (Fig. 5), each with separately tunable output, are used to provide four tunable parameters (Fig. 3).

To achieve the speed required for the RF/IF direct A/D conversion, continuous-time technique based on integrated LC resonators is utilized in this work. The series

connection of two second-order LC resonators yields a fourth order modulator.

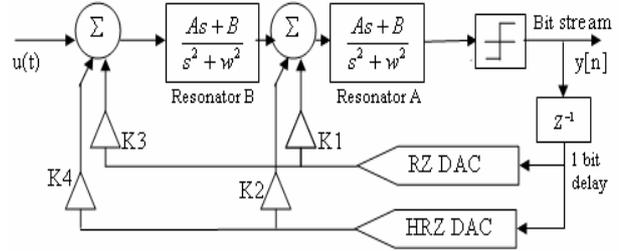


Fig. 3 System level block diagram

However, the integrated inductors have a quite low quality factor, which is only 1.5 at the resonance frequency of 250MHz, so the parasitic series resistors R_s of the on-chip inductors L have to be taken into consideration. To compensate the parasitic effects of the Low-Q inductors, negative resistors $-R$ are connected in parallel with the LC tanks. The equivalent resistance of the overall resonator structure (Fig. 4) is:

$$Z_{eq} = \frac{1}{\frac{1}{sL + R_s} + sC + \frac{1}{-R}} = \frac{\frac{1}{C}s + \frac{R_s}{LC}}{s^2 + s(\frac{R_s}{L} - \frac{R}{C}) + \frac{1}{LC}(1 - \frac{R_s}{R})} \quad (4)$$

The negative resistor is realized by a transconductor, which is tunable to make zero the s term coefficient in the denominator of (4). When $R_s \ll R$, the center frequency of the biquadratic transfer function is verified to be $\omega_0 \approx \frac{1}{\sqrt{LC}}$.

Then, the equation (4) is simplified to the form of $\frac{As+B}{s^2+w^2}$.

This explains why in Fig. 3 the resonators have a low pass term, instead of being purely band pass.

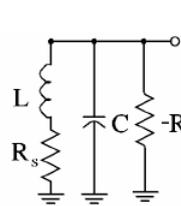


Fig. 4 Resonator structure

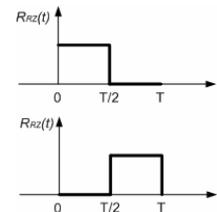


Fig. 5 DAC waveforms

One of the other challenges is the metastability problem. Due to finite circuit regeneration speed, the quantizer circuit needs more time to resolve the polarity of input voltage with smaller magnitude. That is to say, the output waveform $y[n]$ will experience a different delay according to the quantizer input magnitude. This effect is the classic problem of metastability in digital latches [12]. In our case, this type of effect will cause out-of-band noise to fold into the signal band and degrade the converter resolution.

To address the metastability effect, we split the DT prototype $H_{BP4}(z)$ into two parts: z^{-1} and $\frac{2z^{-1} + z^{-3}}{(1 + z^{-2})^2}$, as shown in equation (2). The CT equivalent is found for $\frac{2z^{-1} + z^{-3}}{(1 + z^{-2})^2}$ according to the transformation rule in equation (1), and the one sample delay z^{-1} is introduced prior to the DACs (Fig. 3). The one-digital-delay z^{-1} is realized by two latches and these two latches will provide the circuit enough regeneration time to resolve the quantizer input. In the next section, further details on circuit design are given.

3. CIRCUIT DESIGNS

The circuit level design is implemented in a fully differential structure for noise rejection. The block diagram of the circuit is shown in Fig. 6, which is reminiscent of Fig. 3 in style.

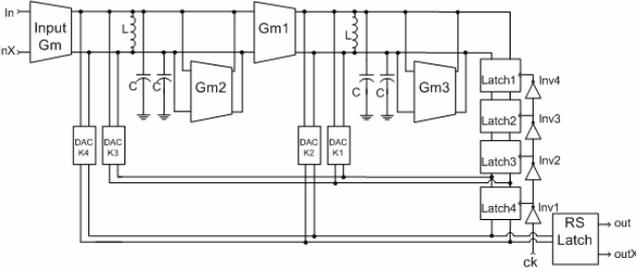


Fig. 6 Block diagram of the circuit design

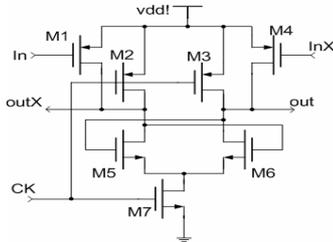


Fig. 7 Circuit of the RZ latch

During the implementation, the quantizer and one-digital-delay z^{-1} , as well as the RZ and HRZ DACs, are combined together. They are realized by four identically structured RZ latches. Fig. 7 shows the circuit diagram of these latches. When the clock voltage is high, the voltage difference between the input pins is amplified to “vdd-vs-gnd” at the output by the cross coupled pair of M5 and M6. During the other half period when the clock is low, M7 is off, while M2 and M3 reset both output to a high voltage. Latch 1 serves as a quantizer by resolving its input and gives a RZ output waveform. The other latches are clocked on the inverted clock phase from their previous stage, so that they will provide a half-sample delay each. In this way, the voltage outputs of latch 3 and latch 4 become one-digital-delayed RZ and one-digital-delayed HRZ waveforms respectively.

However, excess loop delay [13] needs to be taken care of here. It is the delay in the feedback waveform due to finite transition time of the transistors in latches and DACs. It will alter the mapping between the CT system and its DT prototype, if not designed for. In our design, the excess loop delay is compensated by a delay in the clock signal, which is introduced by the inverter series to make the clock signals for latch 3 and 4 slightly ahead of those for latch 1 and 2.

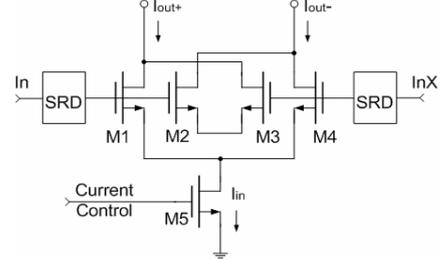


Fig. 8 DAC circuit diagram

The voltage output waveforms of latch 3 and latch 4 are fed back to the modulator by summing in the current domain. DACs of K1 to K4 are used to do the voltage-to-current conversion. They are also used to tune the feedback coefficients as described in Fig. 3 by adjusting their current sources. These DACs are implemented as simple tunable current switches (Fig. 8). M2 and M3 are dummy transistors to cancel out the feed-through charges from the gates. A Swing-Reduction-Driver (SRD) is included at each voltage input to reduce the input voltage swing. It can minimize the clock feed-through and increase the switching speed by reducing the charges transferred.

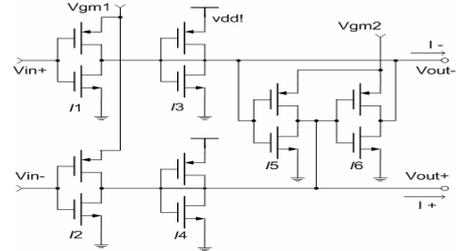


Fig. 9 Circuit diagram of transconductors

The transconductor used in the modulator is based on the structure first proposed by Nauta in [14]. Readers are recommended to refer to the original works [14][15] for a thorough analysis. The circuit diagram is shown in Fig. 9. Being based on inverters, this transconductor structure is well suited for high speed operations up to gigahertz. The inverter pair of I1 and I2 is used as Gm1 (or the input Gm) in Fig. 6, while the inverters I3 and I4 guarantee the common-mode stability. The inverter pair of I5 and I6 is equivalent to Gm2 (or Gm3) to realize the negative resistance for Q-enhancement of the on-chip inductor. Vgm1 and Vgm2 are control voltages for fine tuning the transconductors.

4. SIMULATION RESULTS

The bandpass delta sigma modulator is implemented in a 0.35 μ m triple-metal standard analog CMOS technology. The full layout of circuit design is shown in Fig. 10. The modulator occupies about 1.0 mm², with the two on-chip inductors consuming about 60% of the total area. Post-layout simulation is done in CADENCE design environment with the simulator SPECTRE. The power dissipation is 434 mW from a 3.3V single power supply. The frequency spectrum of the captured bit stream of modulator output is shown in Fig. 11. As we can see from the simulation result, the quantization noise is shaped away from the signal band which is located around 250MHz. Fig. 12 shows the simulated Signal-to-Noise-and-Distortion Ratio (SNDR) for different input levels. In a 15.6MHz bandwidth corresponding to an over-sampling ratio of 64, the modulator achieves a maximum SNDR of 46.86dB, which is equivalent to 7.5 bits of resolution.

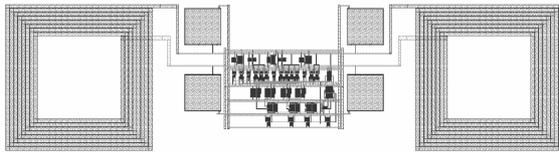


Fig. 10 Full circuit layout

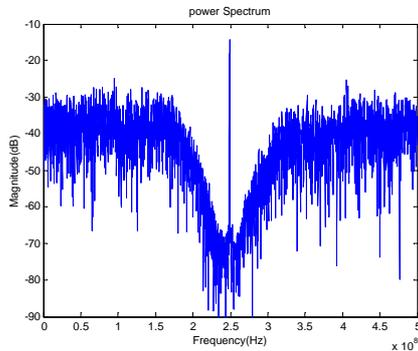


Fig. 11 Frequency spectrum of captured output bit stream

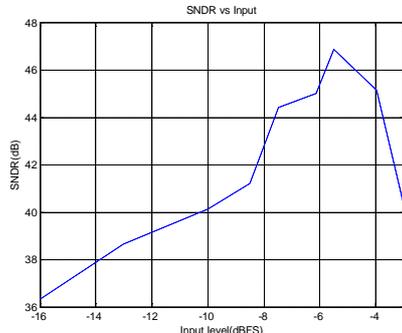


Fig. 12 SNDR vs. input level

5. CONCLUSION

In this paper, we have presented the design of a fourth-order bandpass continuous-time delta sigma modulator. The center frequency of the bandpass signal is greatly pushed from tens of megahertz to 250 MHz for standard CMOS technologies. If the same circuit is implemented in a more advanced submicron process, the modulator frequency can be pushed further. This design offers a low cost way to realize high-speed A/D converters.

6. REFERENCES

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