# Appendix H
# Derivation of Rule Limiting Open Circuit Board Area

This appendix contains equations that describe the rationale for the internal charging design guideline in Section 3.2.3.2.6, Fill Circuit Board Material with Grounded/Referenced Metal, that limits open volumes on a standard circuit board to less than 0.3 $cm^2$. The assumptions and resulting design guideline presented in this appendix have not been validated by test.

This derivation has been approached as a volumetric equation, i.e., the threat is developed on the basis that, when a surface area is dielectric, the circuit board under that dielectric is also a dielectric through to the bottom with no ground planes or traces to interrupt the storage of undesired energy in that volume. If there were a ground plane at some depth, these calculations estimate a greater storage of energy than actually would be present.

The new rule additionally allows for the presence of ground planes, which reduces the level of concern. The energy of a capacitor of area A and discharge voltage V is:

$$E = \frac{1}{2} C V^2 \tag{H-1}$$

where:

$E$ = joule

$C$ = farad

$V$ = volt

This capacitor is based on FR4 circuit board material with a relative dielectric constant of 4.7 and a 1 cm × 1 cm × ~2 mm (80 mil) thick patch with a 2000 V discharge voltage. The capacitor contains about $2 \times 10^{10}$ electrons. This quantity of electrons per square cm is the amount believed to be critical for internal discharges. The resultant calculated stored energy is about 4 μJ. The design rule is based on protection of a victim with an assumed 1 μJ damage sensitivity so there should be a limit of approximately 0.3 $cm^2$ for area of an empty circuit board region. Extending the equation:

$$C = \varepsilon_O \times \varepsilon_r \times A/t \qquad \text{(H-2)}$$

where:

$\varepsilon_O \times \varepsilon_r$ = permittivity of the capacitance material

$t$ = thickness of the capacitor

If the potential of the discharge voltage is adjusted to be proportional to the thickness (V = k × t) and the results of the equations are combined:

$$E = 0.5 \times (\varepsilon_O \times \varepsilon_r \times A/t) \times (k \times t)^2 \qquad \text{(H-3)}$$

or

$$E = 0.5 \times (\varepsilon_O \times \varepsilon_r \times A) \times (k^2) \times t \qquad \text{(H-4)}$$

where:

$k$ = dielectric strength (V/m, for example) for the material in question.

The number of electrons implicit in this equation is the same, but the available energy to damage components is proportional to the thickness. If a ground plane (or power plane) is 8 mil below the dielectric surface, the stored energy will be less than a ground plane at 20 mil depth, in proportion to the dielectric thickness, which reduces the level of concern. The ground (or power) plane provides a nearby conductive medium to leak off charge during the charging process. During the discharge process, it provides a nearby location for the discharge to strike and is a much more robust victim than an IC.

A clarification of the rule is that it was based on an assumption that the material in question is approximately square. If it is a long thin area, it is more difficult to concentrate the ESD energy in one pulse. Therefore, the applicable aspect ratio is 3:1. That is, the rule will permit a long patch of dielectric if one dimension is less than 0.3 cm (3 mm).

This effect is shown in Fig. H-1 (same as Fig. 3-1), which also proposes a new rule for exposed dielectric areas on circuit boards. The design rule assumes a standard FR4 circuit board material of 80 mil (~2 mm) thickness.

An experiment was performed to determine energy transfer from an area of circuit board metal to a victim wire [1]. The energy transferred from a charged metal area of 1 $cm^2$ at breakdown to a nearby trace on the circuit board into a 50 Ω load was ~0.5 μJ, roughly one-tenth the amount calculated above for energy stored in a dielectric volume of the same 1 $cm^2$ surface area on the 80 mil thick dielectric. This might indicate a 10 percent energy transfer efficiency. It provides a rough validation of the analytic results derived above.

## References

[1] P. L. Leung, G. H. Plamp, and P. A. Robinson, Jr., "Galileo Internal Electrostatic Discharge Program," S*pacecraft Environmental Interactions Technology 1983*, October 4-6, Colorado Springs, Colorado, NASA CP-2359/AFGL-TR-85-0018, National Aeronautics and Space Administration, pp. 423-435, 1983.
This paper, documented in the 1985 publication and presented at the *4th Spacecraft Charging Technology Conference*, describes a very neat and clear test that measures the effect of line lengths and circuit board metal areas in the resultant ESD amplitude. It also measures the amplitude of ESD transients from electron beam charging on 50 Ω loads from various conductors.

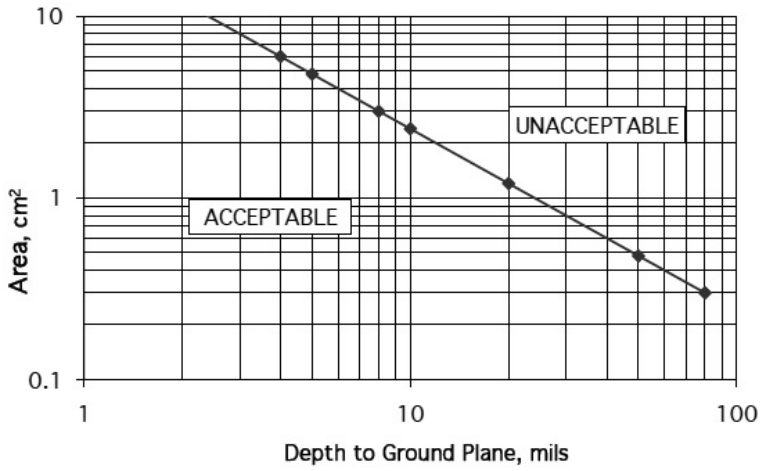


**Fig. H-1. Permissible open area of 80 mil thick FR4 circuit board material versus depth to a ground plane or power plane (preferred) or other circuit traces.**